

Digital Modulator Employing a Polyphase Up-Converter Structure**ABSTRACT**

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An upconverting circuit is disclosed. The upconverting circuit includes a polyphase component generator that provides N_p polyphase components at each input polyphase cycle, wherein $N_p > 2$ on each input polyphase cycle defined by a clock. A memory stores the polyphase components from at least one polyphase cycle prior to the current polyphase cycle.

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A plurality of filters process the polyphase components stored in the memory. Each filter processes a plurality of the polyphase components to generate a filtered polyphase component corresponding to that filter. A multiplexer outputs the filtered polyphase components in a predetermined order to generate a filtered output signal. In one embodiment, each filter

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utilizes the same functional relationship to generate the filtered polyphase components. In another embodiment, the memory is a shift register. The filters can be of arbitrary complexity.